



## UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

## NOTICE OF ALLOWANCE AND FEE(S) DUE

116

7590

02/04/2010

PEARNE & GORDON LLP  
1801 EAST 9TH STREET  
SUITE 1200  
CLEVELAND, OH 44114-3108

EXAMINER

PATEL, NITIN

ART UNIT

PAPER NUMBER

2629

DATE MAILED: 02/04/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/587,632	09/14/2006	Xiao-Yang Huang	36398U/S1	1211
TITLE OF INVENTION: STACKED DISPLAY WITH SHARED ELECTRODE ADDRESSING				

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	05/04/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. **PROSECUTION ON THE MERITS IS CLOSED.** THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN **THREE MONTHS** FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. **THIS STATUTORY PERIOD CANNOT BE EXTENDED.** SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

## HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER:** Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

# **PART B - FEE(S) TRANSMITTAL**

**Complete and send this form, together with applicable fee(s), to:** Mail **Mail Stop ISSUE FEE**  
**Commissioner for Patents**  
**P.O. Box 1450**  
**Alexandria, Virginia 22313-1450**  
**or Fax** **(571)-273-2885**

**INSTRUCTIONS:** This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

116 7590 02/04/2010

**PEARNE & GORDON LLP**  
**1801 EAST 9TH STREET**  
**SUITE 1200**  
**CLEVELAND, OH 44114-3108**

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

## **Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/587,632	09/14/2006	Xiao-Yang Huang	36398U/S1	1211
TITLE OF INVENTION: STACKED DISPLAY WITH SHARED ELECTRODE ADDRESSING				

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	05/04/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
PATEL, NITIN	2629	345-087000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a **Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

1

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2

3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY AND STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee  
☐ Publication Fee (No small entity discount permitted)  
☐ Advance Order - # of Copies \_\_\_\_\_

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.  
☐ Payment by credit card. Form PTO-2038 is attached.  
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number \_\_\_\_\_ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature \_\_\_\_\_ Date \_\_\_\_\_

Typed or printed name \_\_\_\_\_ Registration No. \_\_\_\_\_

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/587,632	09/14/2006	Xiao-Yang Huang	363981US1	1211
116 7590 02/04/2010			EXAMINER	
PEARNE & GORDON LLP 1801 EAST 9TH STREET SUITE 1200 CLEVELAND, OH 44114-3108			PATEL, NEVIN	
			ART UNIT	PAPER NUMBER
			2629	

DATE MAILED: 02/04/2010

## Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 630 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 630 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

**Notice of Allowability****Application No.**

10/587,632

**Applicant(s)**

HUANG ET AL.

**Examiner**

Nitin Patel

**Art Unit**

2629

**- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 10/22/2009.
2. ☒ The allowed claim(s) is/are 1-48.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some\* c) ☐ None of the:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.  
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached  
1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.  
(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.  
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-946)
3. ☐ Information Disclosure Statements (PTO/SB/08),  
Paper No./Mail Date \_\_\_\_\_
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413)  
Paper No./Mail Date \_\_\_\_\_
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_.

/Nitin Patel/  
Primary Examiner, Art Unit 2629

### REASON FOR ALLOWANCE

1. Claims 1-48 are allowed.
2. The following is an examiner's statement of reason for allowance:

The subject matter of the independent claims could either not be found or was not suggested in the prior art of record. The subject matter not found was a liquid crystal display having a plurality of stacked layers comprising: a plurality of layers of liquid crystal material each having opposing surfaces; a plurality of electrically conductive layers disposed so as to be located near both of said opposing surfaces of said liquid crystal layers, wherein each pair of adjacent liquid crystal layers has exactly one of said electrically conductive layers is disposed between the pair adjacent said liquid crystal layers, and drive electronics adapted to apply the voltage pulses to each of the pair of adjacent said liquid crystal layers along the only one said electrically conductive layer provided between the pair of adjacent liquid crystal layers for driving both of the pair of adjacent liquid crystal layers as claimed in claim 1.

A stacked liquid crystal display sequentially comprising the following stacked layers: a top electrode layer of electrodes; a first liquid crystal layer; an upper middle electrode layer of electrodes; a second liquid crystal layer; a lower middle electrode layer of electrodes; a third liquid crystal layer; a bottom electrode layer of electrodes, and a shared electrode addressing construction in which said upper middle electrode layer is adapted to enable driving of said first liquid crystal layer and said second liquid crystal layer and said lower middle electrode layer is adapted to enable driving of said second liquid crystal layer and said third liquid crystal layer as claimed in claim 9. and

adapted such that a reflective state of a portion said first liquid crystal layer corresponding to a pixel of said display is changed by providing a voltage difference between an electrode of said top electrode layer and an electrode of said upper middle electrode layer, and adapted such that a reflective state of a portion said second liquid crystal layer corresponding to said pixel of said display is changed by providing a voltage difference between an electrode of said upper middle electrode layer and an electrode of said lower middle electrode layer, and further adapted such that a reflective state of a portion of said third liquid crystal layer corresponding to said pixel of said display is changed by providing a voltage difference between an electrode of said lower middle electrode layer and an electrode of said bottom electrode layer; thereby updating a state of said pixel of said display as claimed in claim 17.

A stacked liquid crystal display comprising: a top electrode layer of electrodes; an upper middle electrode layer of electrodes; a first liquid crystal layer sandwiched between said top electrode layer and said upper middle electrode layer; a lower middle electrode layer of electrodes; a second liquid crystal layer sandwiched between said upper middle electrode layer and said lower middle electrode layer; a bottom electrode layer of electrodes; a third liquid crystal layer sandwiched between said lower middle electrode layer and said bottom electrode layer; wherein a pixel of said display includes a portion of said first liquid crystal layer adapted to be addressed by the combination of an electrode of said top electrode layer and an electrode of said upper middle electrode layer, and wherein said pixel of said display further includes a portion of said second liquid crystal layer adapted to be addressed by the combination of an electrode of said

upper middle electrode layer and an electrode of said lower middle electrode layer, and further wherein said pixel of said display further includes a portion of said third liquid crystal layer adapted to be addressed by the combination of an electrode of said lower middle electrode layer and an electrode of said bottom electrode layer as claimed in claim 22.

A stacked liquid crystal display comprising: a top electrode layer of electrodes; an upper middle electrode layer of electrodes; a first liquid crystal layer sandwiched between said top electrode layer and said upper middle electrode layer, adapted such that a brightness state of a portion said first liquid crystal layer corresponding to a pixel of said display is changed by providing a non-zero voltage difference between an electrode of said top electrode layer and an electrode of said upper middle electrode layer, and adapted such that a brightness state of said portion of said first liquid crystal layer is maintained by providing substantially no voltage difference between said electrode of said top electrode layer and said electrode of said upper middle electrode layer; a lower middle electrode layer of electrodes; a second liquid crystal layer sandwiched between said upper middle electrode layer and said lower middle electrode layer, adapted such that a brightness state of a portion said second liquid crystal layer corresponding to said pixel of said display is changed by providing a non-zero voltage difference between an electrode of said upper middle electrode layer and an electrode of said lower middle electrode layer, and adapted such that a brightness state of said portion of said second liquid crystal layer is maintained by providing substantially no voltage difference between said electrode of said upper middle electrode layer and said

electrode of said lower middle electrode layer; a bottom electrode layer of electrodes; and a third liquid crystal layer sandwiched between said lower middle electrode layer and said bottom electrode layer, adapted such that a brightness state of a portion of said third liquid crystal layer corresponding to said pixel of said display is changed by providing a non-zero voltage difference between an electrode of said lower middle electrode layer and an electrode of said bottom electrode layer, and adapted such that a brightness state of said portion of said third liquid crystal layer is maintained by providing substantially no voltage difference between said electrode of said lower middle electrode layer and said electrode of said bottom electrode layer; wherein said pixel is formed by a stacked arrangement of said portions of said first, second, and third liquid crystal layers such that a color of said pixel is formed by light reflecting from all of said portions of said first, second, and third liquid crystal layers, and further wherein a brightness state of said pixel of said display is updated by changing and/or maintaining the brightness states of said portions of said first, second, and third liquid crystal layers sequentially or concurrently as claimed in claim 24.

A multi-layer stacked liquid crystal display film comprising: a plurality of liquid crystal film layers; and a plurality of electrode film layers for driving said plurality of liquid crystal film layers, wherein all of said film layers are printed or coated in a stack upon each other, wherein a pixel is formed from a portion of each of said plurality of liquid crystal layers, such that a color or shade of said pixel is formed by light reflecting from all of said portions of said plurality of liquid crystal layers, and wherein at least one of



said plurality of electrode layers is adapted to enable driving of two adjacent said liquid crystal layers as claimed in claim 26.

A stacked liquid crystal display comprising a base substrate and a plurality of film layers printed or coated onto each other in a stack and supported on said substrate, said film layers comprising: a plurality of conducting film layers; and a plurality of liquid crystal dispersion film layers each comprising regions of liquid crystal material dispersed in a polymer matrix, said liquid crystal dispersion layers being separated by said conducting layers, wherein at least one of said plurality of conducting layers is adapted to enable driving of two adjacent said liquid crystal dispersion layers as claimed in claim 28.

A liquid crystal display comprising: a first liquid crystal layer comprising liquid crystal that is bistable in an absence of an electric field; a second liquid crystal layer comprising liquid crystal that is bistable in an absence of an electric field stacked upon said first liquid crystal layer, wherein said liquid crystal is a dispersion of liquid crystal in a polymer matrix; a first electrode layer disposed between said first liquid crystal layer and said second liquid crystal layer; a second electrode layer disposed between said first liquid crystal layer and said second liquid crystal layer; electrical interconnects that electrically connect said first electrode layer and said second electrode layer together in parallel; and drive electronics electrically connected to said electrical interconnects adapted to address both of said first liquid crystal layer and said second liquid crystal layer with the same voltage pulses as claimed in claim 32.

A liquid crystal display comprising: a first liquid crystal layer comprising liquid crystal that is bistable in an absence of an electric field; a second liquid crystal layer comprising liquid crystal that is bistable in an absence of an electric field stacked upon said first liquid crystal layer, wherein said first liquid crystal layer and said second liquid crystal layer comprise a dispersion of bistable cholesteric liquid crystal material in a polymer matrix; only a single electrode layer disposed between said first liquid crystal layer and said second liquid crystal layer; and drive electronics electrically connected to said single electrode layer adapted to address both said first liquid crystal layer and said second liquid crystal layer with the same voltage pulses as claimed in claim 34.

A liquid crystal display comprising: a first liquid crystal layer comprising liquid crystal that is bistable in an absence of an electric field; a second liquid crystal layer comprising liquid crystal that is bistable in an absence of an electric field stacked upon said first liquid crystal layer, wherein said first liquid crystal layer and said second liquid crystal layer comprise a dispersion of bistable cholesteric liquid crystal material in a polymer matrix; only a single electrode layer disposed between said first liquid crystal layer and said second liquid crystal layer; and drive electronics electrically connected to said single electrode layer adapted to address both said first liquid crystal layer and said second liquid crystal layer with the same voltage pulses as claimed in claim 34.

A liquid crystal display having a plurality of stacked layers comprising: a plurality of layers of liquid crystal material; and a plurality of layers of electrodes such that each of said plurality of layers of liquid crystal material is adjacent to exactly two of said plurality of layers of electrodes, wherein each one of said electrode layers provided

between and adjacent to two layers of liquid crystal material is used to drive each one of said adjacent layers of liquid crystal material as claimed in claim 43.

A liquid crystal display having a plurality of stacked layers comprising: a plurality of layers of liquid crystal material; and a plurality of layers of electrodes such that each of said plurality of layers of liquid crystal material is adjacent to exactly two of said plurality of layers of electrodes, wherein each one of said pixel is comprised of plurality of sub-pixels, wherein each one of said sub-pixels is provided by one of said layers of liquid crystal material, and wherein each pixel is driven by selectively driving, in sequence, each one of its corresponding sub-pixels one at a time while simultaneously deslecting the others of its sub-pixels as claimed in claim 46.

A liquid crystal display having a plurality of stacked layers comprising: a plurality of layers of liquid crystal material each having opposing surfaces and arranged in a stack; a plurality of electrically conductive layers arranged such that one of said electrically conductive layers is at the top of the stack, one of said electrically conductive layers is arranged at the bottom of the stack, and each one of the remainder of said electrically conductive layers is arranged between a different adjacent pair of said layers of liquid crystal material; and drive electronics adapted to drive said display such that each one of said electrically conductive layers that is arranged between a different adjacent pair of the layers of liquid crystal material is utilized to drive both layers of the adjacent pair of layers of liquid crystal material as claimed in claim 47. ...., in combination with the other elements (or steps) of the apparatus and method recited in the claims.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Patel whose telephone number is 571-272-7677. The examiner can normally be reached on 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shalwala Bipin can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nitin Patel/  
Primary Examiner, Art Unit 2629

